20020 28927001

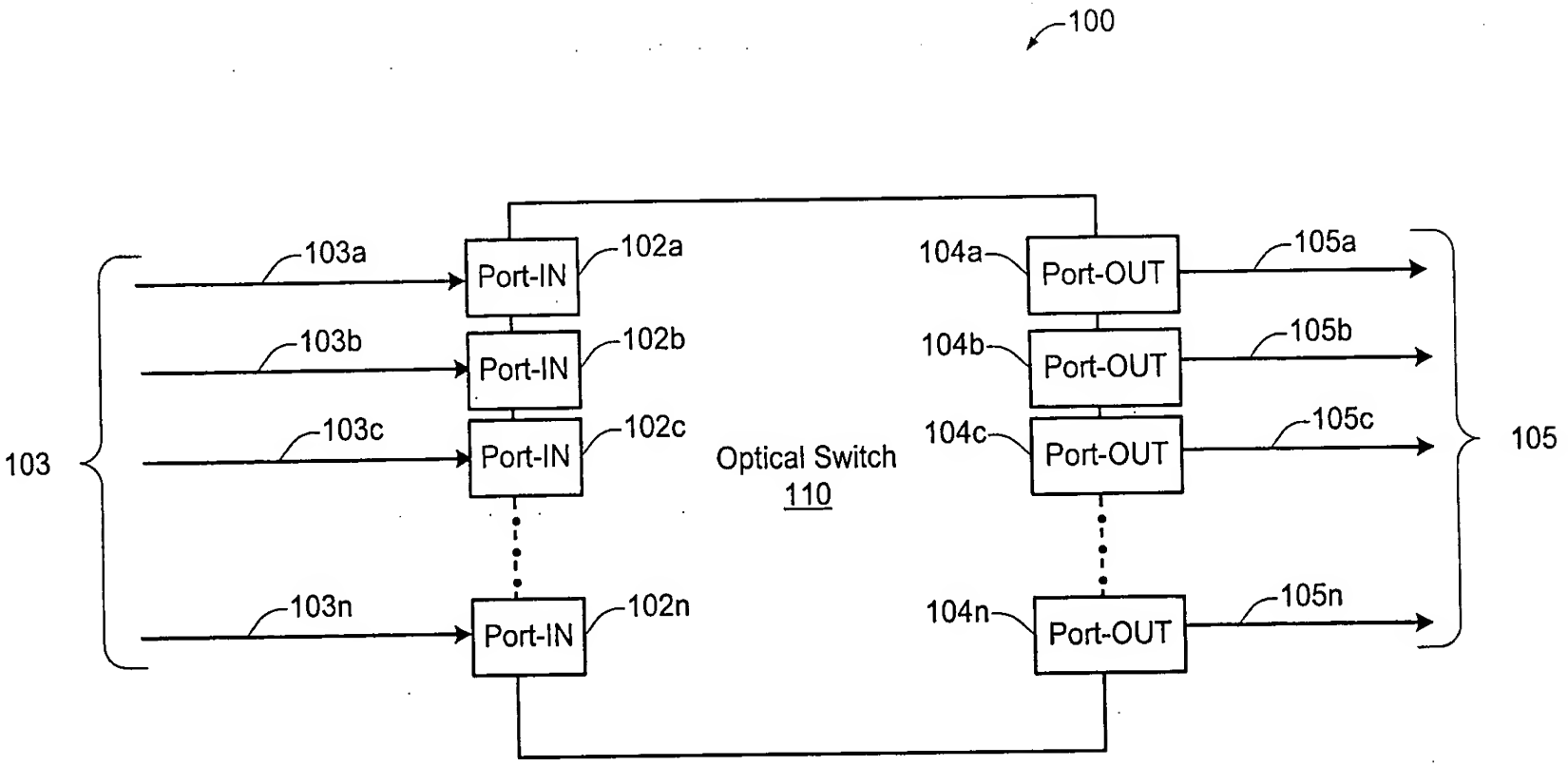


Fig. 1
(Prior Art)

20080208928007

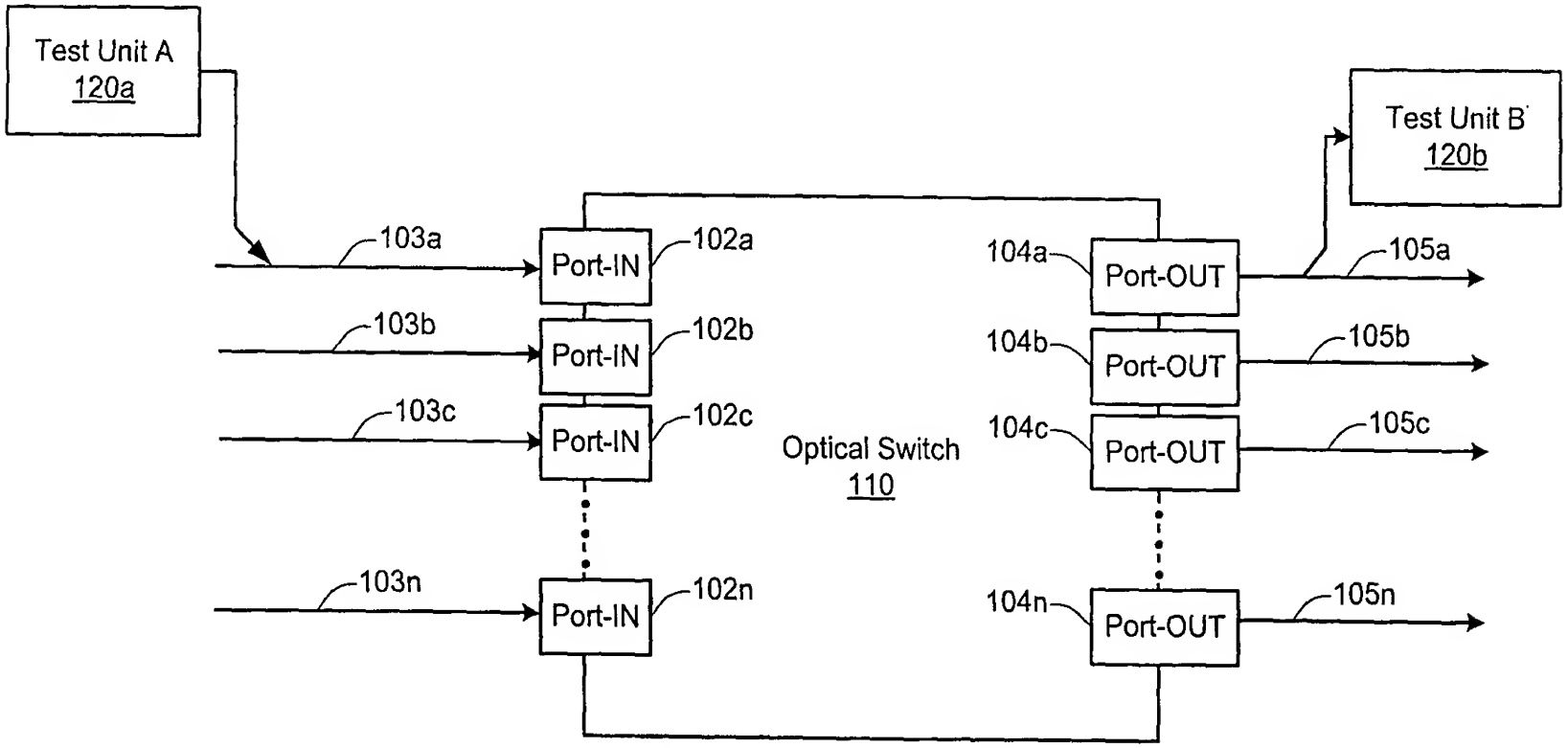


Fig. 2
(Prior Art)

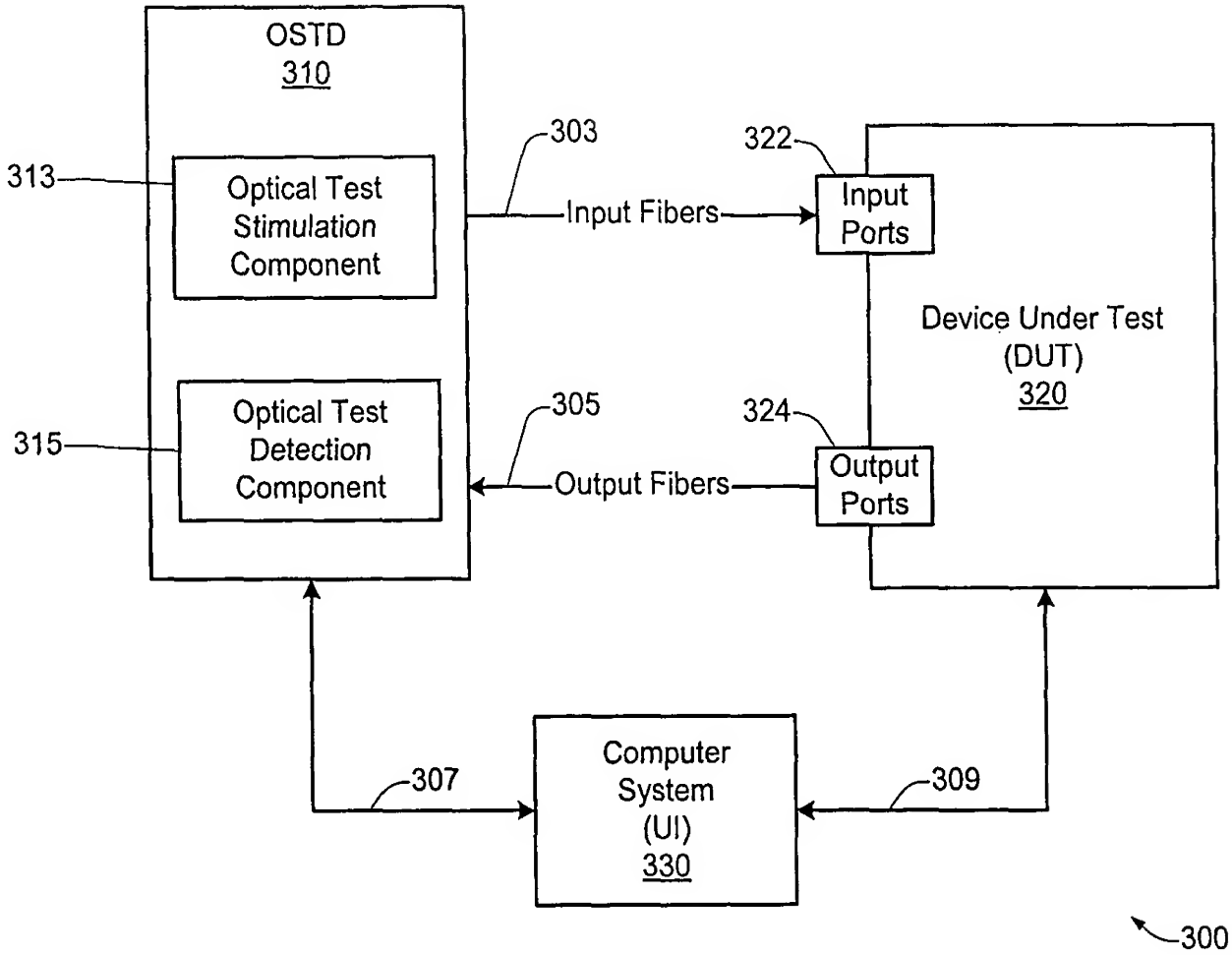

OSTD
310
313
Optical Test
Stimulation
Component
315
Optical Test
Detection
Component
303
Input Fibers
305
Output Fibers
322
Input
Ports
324
Output
Ports
Device Under Test
(DUT)
320
307
309
Computer
System
(UI)
330
300

Fig. 3

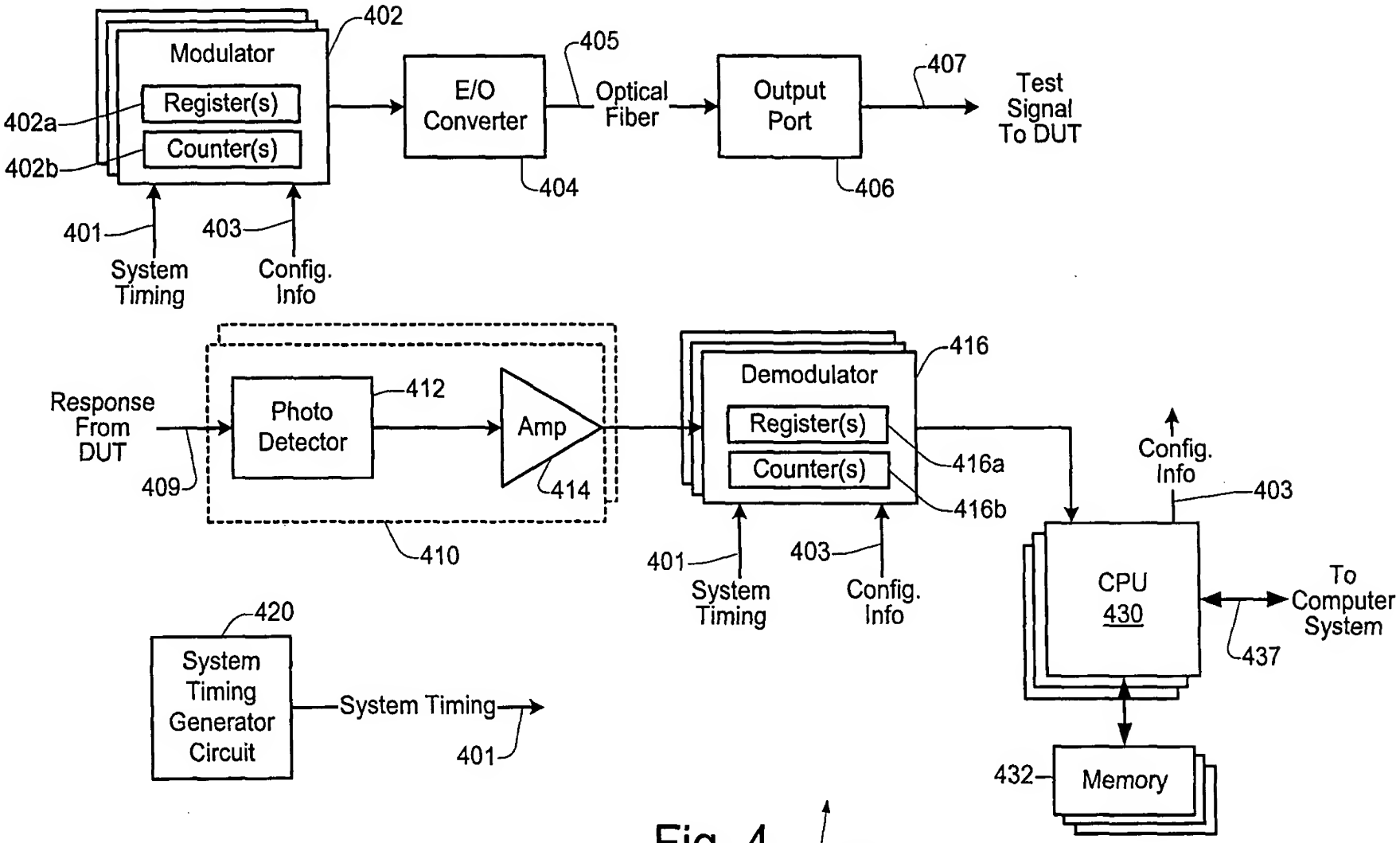
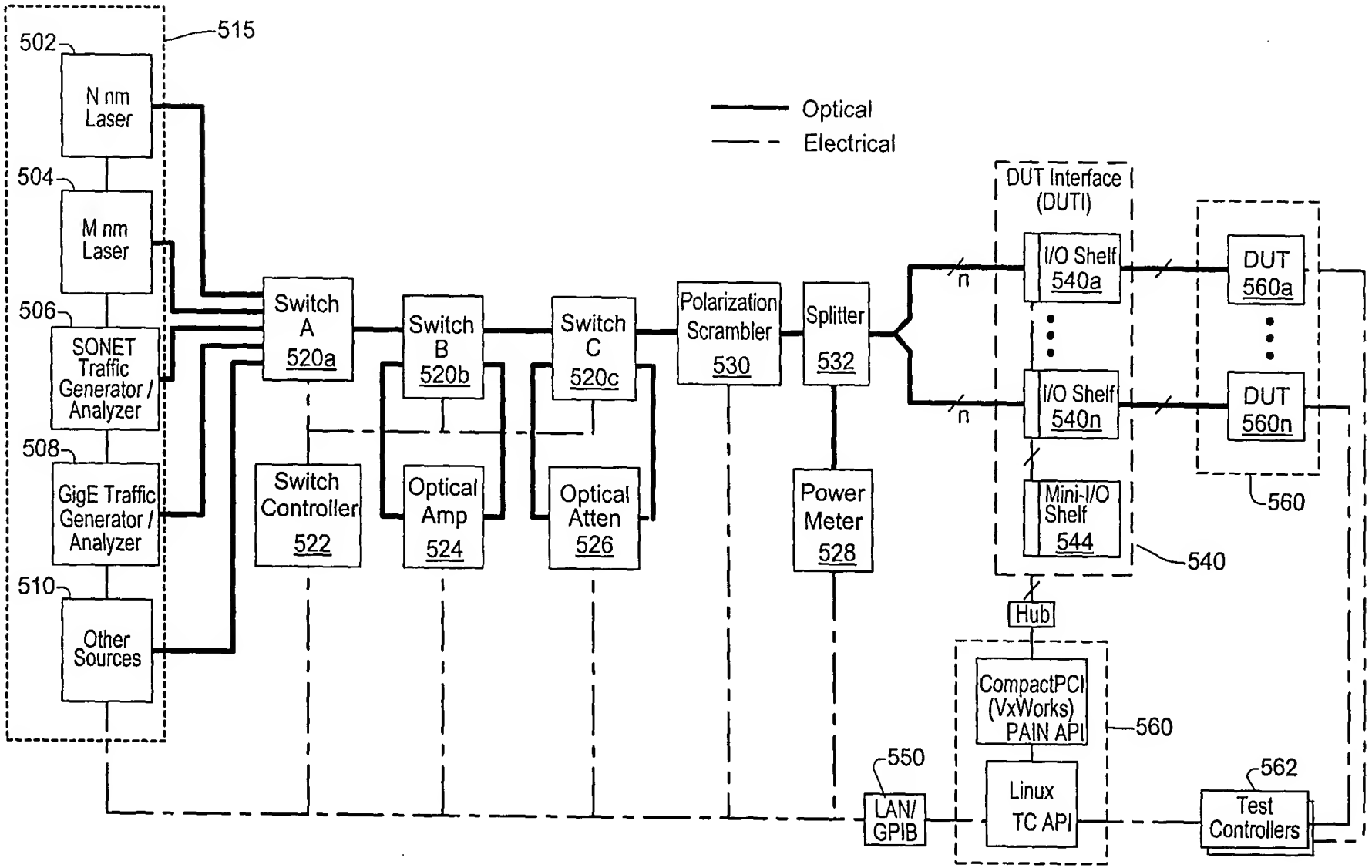

Modulator
Register(s)
Counter(s)
402
402a
402b
E/O Converter
404
405
Optical Fiber
Output Port
406
407
Test Signal To DUT
401
System Timing
403
Config. Info
Response From DUT
409
Photo Detector
412
Amp
414
410
Demodulator
416
Register(s)
Counter(s)
416a
416b
401
System Timing
403
Config. Info
Config. Info
403
CPU
430
To Computer System
437
420
System Timing Generator Circuit
System Timing
401
432
Memory

Fig. 4 400


515
502
N nm Laser
504
M nm Laser
506
SONET Traffic Generator / Analyzer
508
GigE Traffic Generator / Analyzer
510
Other Sources
Optical
Electrical
Switch A 520a
Switch B 520b
Switch C 520c
Polarization Scrambler 530
Splitter 532
Switch Controller 522
Optical Amp 524
Optical Atten 526
Power Meter 528
DUT Interface (DUTI)
I/O Shelf 540a
I/O Shelf 540n
Mini-I/O Shelf 544
540
n
n
DUT 560a
DUT 560n
560
Hub
CompactPCI (VxWorks) PAIN API
560
Linux TC API
550
LAN/ GPIB
562
Test Controllers

500 Fig. 5

1405268v1 - 020202

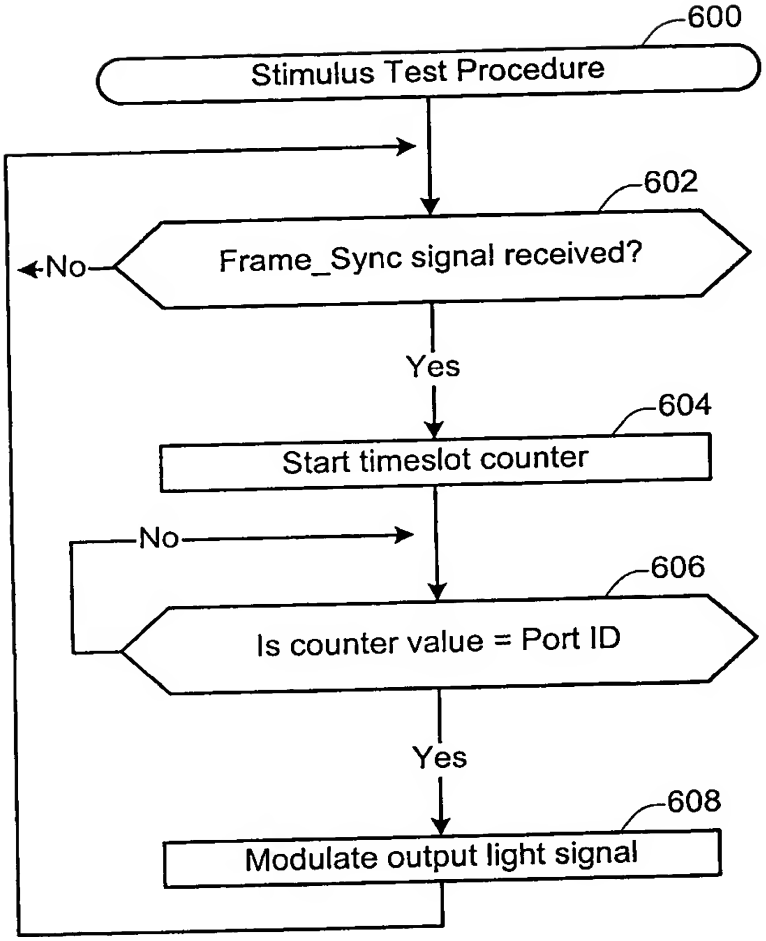


Fig. 6

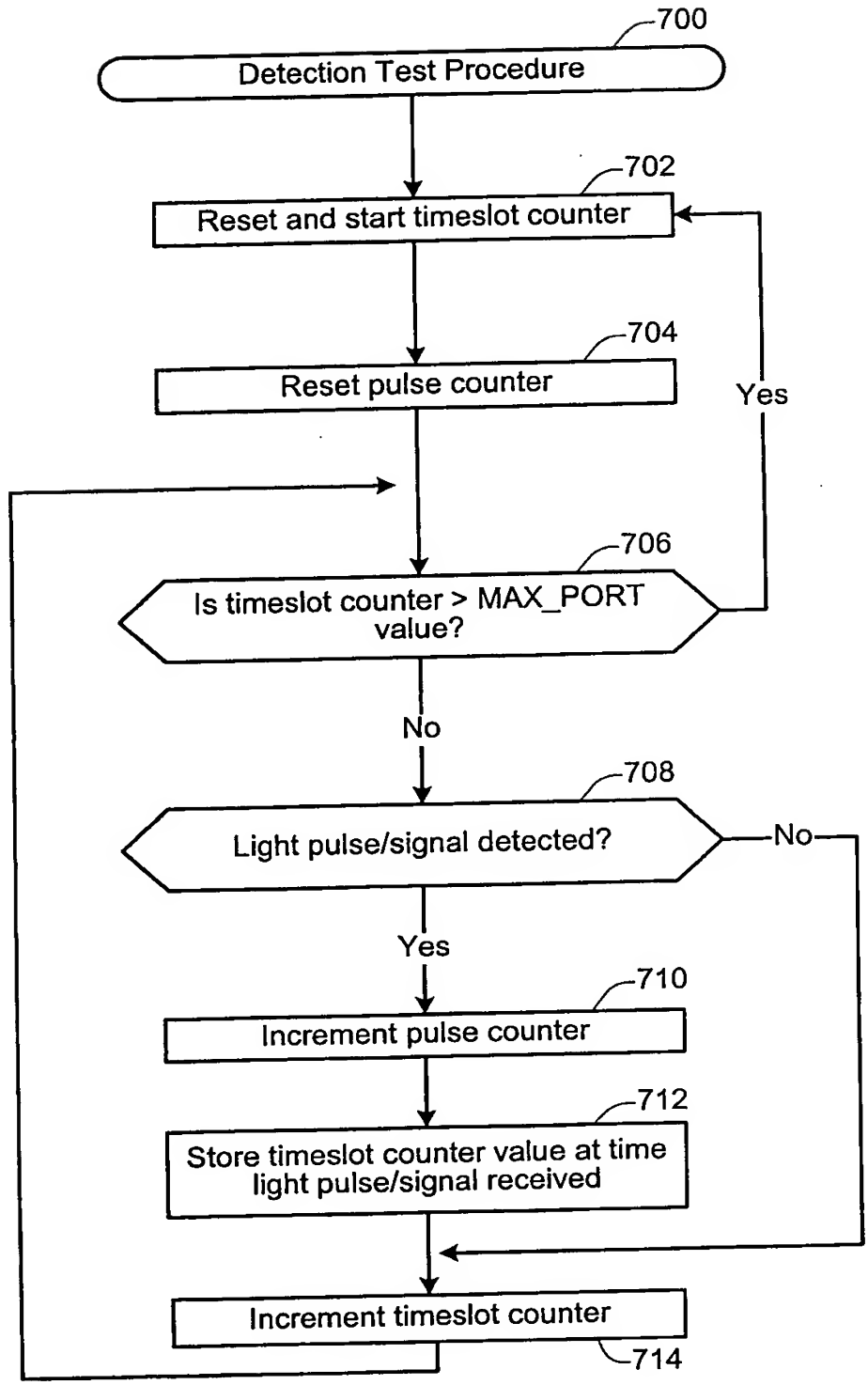

700
Detection Test Procedure
702
Reset and start timeslot counter
704
Reset pulse counter
Yes
706
Is timeslot counter > MAX_PORT value?
No
708
Light pulse/signal detected?
No
Yes
710
Increment pulse counter
712
Store timeslot counter value at time light pulse/signal received
Increment timeslot counter
714

Fig. 7

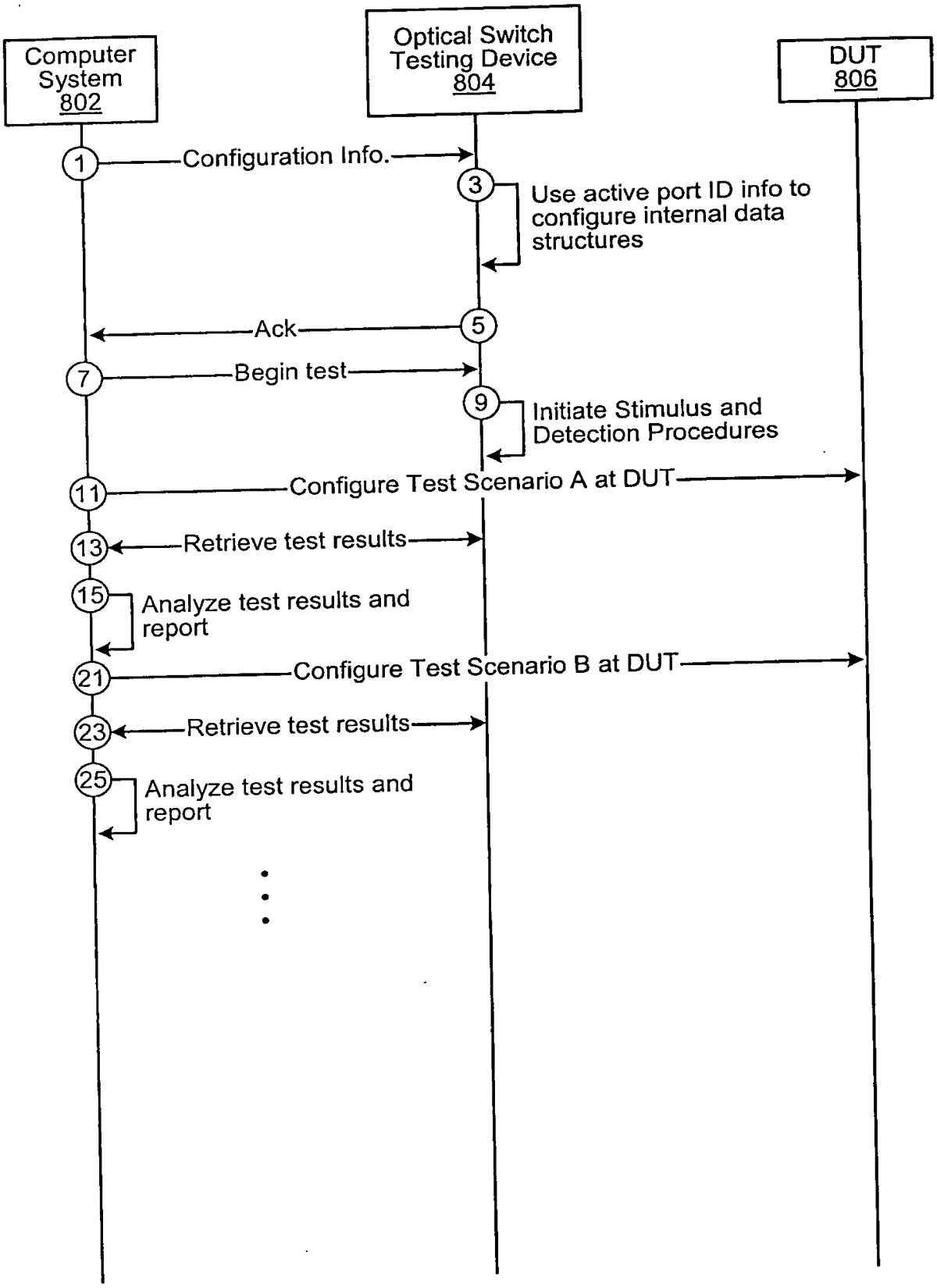

Computer System 802
Optical Switch Testing Device 804
DUT 806
1
Configuration Info.
3
Use active port ID info to configure internal data structures
5
Ack
7
Begin test
9
Initiate Stimulus and Detection Procedures
11
Configure Test Scenario A at DUT
13
Retrieve test results
15
Analyze test results and report
21
Configure Test Scenario B at DUT
23
Retrieve test results
25
Analyze test results and report

Fig. 8

20030207.2892701T

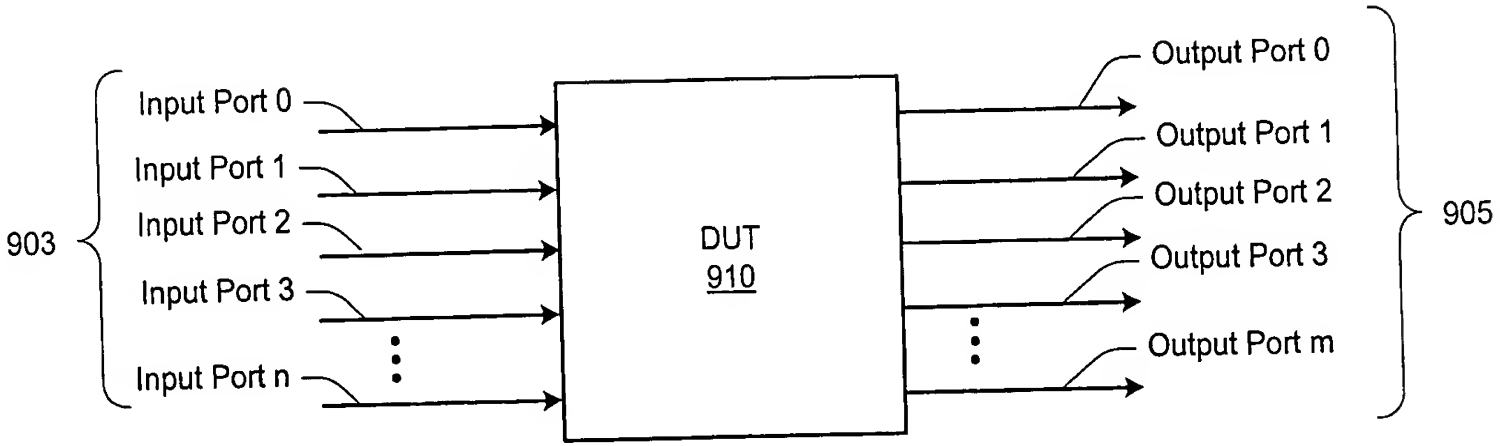


Fig. 9

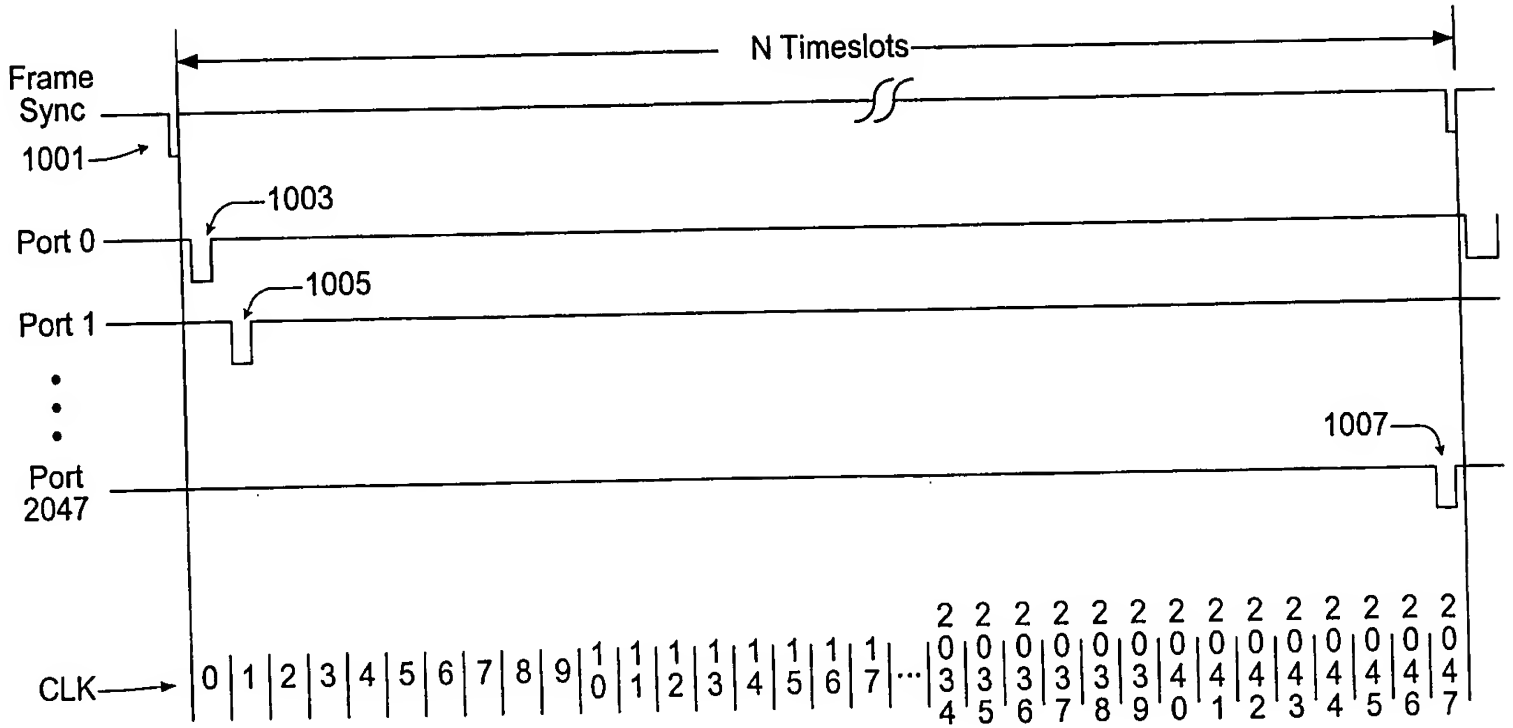

N Timeslots
Frame Sync
1001
1003
Port 0
1005
Port 1
1007
Port 2047
CLK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 ... 2034 2035 2036 2037 2038 2039 2040 2041 2042 2043 2044 2045 2046 2047

Fig. 10

Output Ports
1104

Input Ports 1102	Output Port 0	Output Port 1	Output Port 2	Output Port 3
Input Port 0	Insertion Loss Value A	Insertion Loss Value B	•••	
Input Port 1	Insertion Loss Value C	Insertion Loss Value D	•••	
Input Port 2	Insertion Loss Value E	Insertion Loss Value F	•••	
Input Port 3	⋮	⋮		

Fig. 11A

Output Ports
1104

Input Ports 1102	Output Port 0	Output Port 1	Output Port 2	Output Port 3
Input Port 0	Time Value A	Time Value B	•••	
Input Port 1	Time Value C	Time Value D	•••	
Input Port 2	Time Value E	Time Value F	•••	
Input Port 3	⋮	⋮	⋮	

Fig. 11B